O.P.Code: 20EC0448	R20	H.T.No.									

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)

B.Tech II Year II Semester Regular & Supplementary Examinations June-2024

DIGITAL ELECTRONICS
(Electrical & Electronics Engineering)

Time: 3 Hours **Max. Marks: 60**

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1		Explain about Logic gates. with symbols and truth tables.	CO1	L1	12M
		OR			
2		A receiver with an even parity hamming code receives the data as 1110110. Determine the correct code.	CO1	L3	12M

UNIT-II

3		What are the universal gates? Implement logic gates by using NAND and NOR gates.	CO2	L2	12M
		OR			
4		Simplify the following Boolean expressions using K-map. $F(A, B, C, D)= \pi M(0,2,3,8,9,12,13,15)$	CO2	L3	12M

UNIT-III

5		What is Decoder? Design the circuit for a 3-to-8 decoder with a truth table.	CO4	L1	12M
		OR			
6		What is a parallel adder? Design and explain a 4-bit parallel adder by using a full-adder.	CO4	L3	12M

UNIT-IV

7	a	Explain about level and Edge triggering.	CO5	L1	6M
	b	Explain the operation of series in series out register.	CO5	L1	6M
		OR			
8		With a neat sketch explain 4 bit Johnson counter using D FF.	CO5	L3	12M

UNIT-V

9		Compare three combinational circuits: PLA, PAL and PROM.	CO6	L3	12M
		OR			
10		What is design procedure for FSM? Give the advantages of FSM.	CO6	L3	12M

***** END *****